What is claimed is:

1. A duty cycle correction component comprising:

a differential to single end amplifier that receives a pair of non-corrected sinusoidal signals and generates a pair of corrected square wave signals according to a first pair of adjustment signals and a second pair of adjustment signals;

a cross coupled buffer that buffers the pair of corrected square waves and provides a pair of buffered clock signals; and

a feedback amplifier that receives the pair of buffered clock signals, measures absolute duty cycles of the pair of buffered clock signals, and generates the first and second pairs of adjustment signals according to the measured duty cycles.

2. The component of claim 1, wherein the pair of non-corrected sinusoidal signals include duty cycle distortions.

3. The component of claim 1, wherein the pair of corrected square wave signals have a selected duty cycle of about fifty percent.

4. The component of claim 1, wherein the pair of corrected square wave signals have a selected duty cycle of other than fifty percent.

5. The component of claim 1, wherein the pair of corrected square wave signals comprises a positive square wave signal and a negative square wave signal, wherein the negative square wave signal is complementary to the positive square wave signal.

6. The component of claim 5, wherein the positive square wave signal is

generated from a positive sinusoidal signal of the pair of non-corrected sinusoidal signals according to the first pair of adjustment signals.

7. The component of claim 5, wherein the negative square wave signal is generated from a negative sinusoidal signal of the pair of non-corrected sinusoidal signals according to the second pair of adjustment signals.

8. The component of claim 1, wherein the differential to single end amplifier comprises a pair of AC coupling components that remove DC components from the pair of non-corrected sinusoidal signals to generate a pair of DC decoupled signals.

9. The component of claim 8, wherein the differential to single end amplifier further comprises a pair of biasing components that bias the pair of DC decoupled signals according to a selected duty cycle and the first and second pair of adjustment signals.

10. The component of claim 9, wherein the differential to single end amplifier further comprises a two stage inverter that converts the biased pair of signals to the pair of corrected square wave signals that have about the selected duty cycle.

11. The component of claim 1, wherein the cross coupled buffer comprises a number of stages, wherein respective stages include a pair of cross coupled inverters that at least partially reduce skew from the pair of square wave signals.

12. The component of claim 1, wherein the feedback amplifier measures the absolute duty cycles of the pair of buffered clock signals, compares the measured duty cycles with a desired duty cycle, and generates the two pairs of

adjustment signals according to the comparison.

13. The component of claim 12, wherein the desired duty cycle is about fifty percent.

14. The component of claim 12, wherein the desired duty cycle is other than fifty percent.

15. A portion of a differential to single end amplifier comprising:

an AC coupler that receives an incoming sinusoidal signal and removes DC components from the incoming signal to generate a coupled signal;

a dual stage inverter that converts the coupled signal into a square wave signal with a selected duty cycle; and

a replica bias component that receives a positive adjustment signal and a negative adjustment signal, generates a DC voltage to bias the AC coupled signal to the input of the dual stage inverter according to the threshold of the scaled version of the first stage of the dual stage inverter, the positive adjustment signal, and the negative adjustment signal.

16. The portion of claim 15, wherein the dual stage inverter comprises a first stage that inverts the decoupled signal into an inverted signal and a second stage that inverts the inverted into the square wave signal.

17. A method of generating a corrected duty cycle clock comprising:

generating a pair of differential sinusoidal signals comprising a positive sinusoidal signal and a negative sinusoidal signal;

removing DC components from the pair of differential sinusoidal signals;

biasing the positive sinusoidal signal according to a first pair of adjustment signals;

biasing the negative sinusoidal signal according to a second pair of adjustment signals;

inverting the biased signals into an inverted pair of signals; and

inverting the inverted pair of signals into a differential pair of square waves.

18. The method of claim 17, further comprising measuring a duty cycle of a positive buffered clock signal and generating the first pair of adjustment signals according to the measured duty cycle and a selected duty cycle.

19. The method of claim 18, further comprising measuring a duty cycle of a negative buffered clock signal and generating the second pair of adjustment signals according to the measured duty cycle and the selected duty cycle.

20. The method of claim 19, further comprising buffering the differential pair of square waves to provide the positive buffered clock signal and the negative buffered clock signal.

21. The method of claim 20, further comprising de-skewing the differential pair of square waves.